

WHAT IS CLAIMED IS:

1                   1.       A system for multiplexing data onto a SONET/SDH frame,  
2 comprising:  
3                   a calendar configured to selectively direct input data received from a plurality  
4 of channels;  
5                   a processor configured to receive the input data and process the input data  
6 using virtual concatenation or contiguous concatenation or a combination of both; and  
7                   a terminator configured to terminate overhead data within the SONET/SDH  
8 frame.

1                   2.       The system according to claim 1 wherein the processor is further  
2 configured to handle arbitrary virtual concatenation with STS-1 or STS-3c granularity.

1                   3.       The system according to claim 1 wherein the processor is further  
2 configured to handle contiguous concatenation with STS-Nc capacity, where N is a multiple  
3 of 3.

1                   4.       The system according to claim 1 wherein the processor is further  
2 configured to handle non-standard virtual concatenation and any proprietary concatenation  
3 format.

1                   5.       The system according to claim 1 wherein the processor is configured to  
2 handle mixed concatenation of any contiguous concatenation traffic and virtual concatenation  
3 traffic with STS-3c granularity.

1                   6.       The system according to claim 1 wherein the system is implemented in  
2 a programmable logic device.

1                   7.       The system according to claim 1, wherein the processor is further  
2 configured to receive and process the overhead data; and the system further comprising:  
3                   a shifter configured to redistribute the overhead data and the input data  
4 received from the plurality of channels before the overhead data and the input data are  
5 selectively directed by the calendar to the processor.

1                   8.       The system according to claim 7 wherein the processor is configured to  
2 handle any mixed concatenation including STS-1-Xv.

1                   9.     The system according to claim 1 wherein the overhead data terminated  
2 by the terminator include H1, H2 and H3 bytes in line overhead and H4 byte in path  
3 overhead.

1                   10.    The system according to claim 9 wherein a multi-frame indicator and a  
2 sequence number are inserted into the H4 byte in the path overhead.

1                   11.    A system for multiplexing input data from a plurality of channels onto  
2 a selected one of a plurality of SONET/SDH frames having different sizes, comprising:  
3                   a calendar configured to selectively multiplex the input data received from the  
4 plurality of channels;  
5                   a processor configured to receive the multiplexed input data and re-arrange the  
6 multiplexed input data onto the selected SONET/SDH frame using virtual concatenation or  
7 contiguous concatenation or a combination of both; and  
8                   a terminator configured to terminate overhead bytes within the selected  
9 SONET/SDH frame.

1                   12.    The system according to claim 11 wherein the processor further  
2 comprises:  
3                   an input RAM configured to receive and output the multiplexed input data;  
4                   a crossbar configured to receive and re-arrange the multiplexed input data  
5 outputted from the input RAM;  
6                   an output RAM configured to receive the re-arranged multiplexed data from  
7 the crossbar; and  
8                   a copy machine configured to control and coordinate operation of the input  
9 RAM, the crossbar and the output RAM.

1                   13.    The system according to claim 12 wherein the copy machine is further  
2 configured to control and coordinate the operation of the input RAM, the crossbar and the  
3 output RAM in accordance with a schedule;  
4                   wherein the overhead bytes include sequence numbers; and  
5                   wherein the calendar, the schedule and the sequence numbers are each double  
6 buffered and switched in a predetermined sequence so as to allow hitless re-provisioning.

1                   14.     The system according to claim 12 wherein the copy machine is paused  
2 when the overhead bytes are inserted into the selected SONET/SDH frame.

1                   15.     The system according to claim 12 wherein the input RAM comprises a  
2 plurality of memory banks.

1                   16.     The system according to claim 12 wherein the input RAM is triple  
2 buffered thereby allowing the system to support a fixed latency from data request to data  
3 available.

1                   17.     The system according to claim 16 wherein the fixed latency is up to N  
2 cycles for STS-N traffic.

1                   18.     The system according to claim 11 wherein the processor is further  
2 configured to handle arbitrary virtual concatenation with STS-1 or STS-3 granularity.

1                   19.     The system according to claim 11 wherein the processor is further  
2 configured to handle contiguous concatenation with STS-Nc capacity, where N is a multiple  
3 of 3.

1                   20.     The system according to claim 11 wherein the processor is further  
2 configured to handle non-standard virtual concatenation and any proprietary concatenation  
3 format.

1                   21.     The system according to claim 11 wherein the processor is configured  
2 to handle mixed concatenation of any contiguous concatenation traffic and virtual  
3 concatenation traffic with STS-3c granularity.

1                   22.     The system according to claim 11 wherein the system is implemented  
2 in a programmable logic device.

1                   23.     The system according to claim 11 wherein the processor is further  
2 configured to receive and process the overhead bytes; and the system further comprising:  
3                   a shifter configured to redistribute the overhead bytes and the input data  
4 received from the plurality of channels before the overhead bytes and the input data are  
5 selectively directed by the calendar to the processor.

1                   24.    The system according to claim 23 wherein the processor is configured  
2 to handle any mixed concatenation including STS-1-Xv.

1                   25.    The system according to claim 11 wherein the overhead bytes  
2 terminated by the terminator include H1, H2 and H3 bytes in line overhead and H4 byte in  
3 path overhead.

1                   26.    The system according to claim 25 wherein a multi-frame indicator and  
2 a sequence number are inserted into the H4 byte in the path overhead.

1                   27.    The system according to claim 11 wherein the different sizes of the  
2 plurality of SONET/SDH frames include STS-12, STS-48, STS-192 and STS-768.